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Surface modification and the switching processes in ferroelectric liquid crystals

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This work relates to the control of switching in ferroelectric liquid crystal devices. By considering the various parameters which influence the switching process a method of engineering both the location and threshold of domain nucleation sites has been developed. We have found that deliberate modification of the surface morphology has a profound influence on the domain switching process. This paper discusses the experimental cell construction and switching results.

1. Introduction

The switching processes in ferroelectric liquid crystal C2 aligned devices are now reasonably well understood [1, 2]. On application of an electric field the director (or molecular axis) reorients into a stressed state, where the point at the chevron cusp is pinned and reorientation in the two halves of the device is similar. Then, at certain regions within the device, the director at the chevron cusp flips into the opposite allowed orientation (cone intersections) and domains of the opposite switched state form. These then grow and coalesce until the device (or addressed pixel) has switched completely. Removal of the field during this switching process leaves the device in a multi-domain or partially switched state. This process leads to what can be termed a 'partial switching width' in ferroelectric liquid crystals (figure 1).

Thus, depending on the amplitude and duration of applied switching pulses, a range of final switched area can be obtained. Small pulses will not change the initial state, although the transmission through a device will be momentarily influenced. This case is represented by the 'no switching' region in figure 1. Larger pulses will cause partial switching, with the final switched area depending on the pulse amplitude and duration. With sufficiently large pulses complete switching will take place, and this will be so for all pulses of larger amplitude, unless reverse ('bouncy') switching begins to take place due to ionic effects [3].

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2. The issue

In reference to figure 1, the boundary between the 'no switching' and 'partial switching' regions represents the maximum amplitude pulse which will not cause switching, and the boundary between 'partial switching' and 'full switching' represents the minimum amplitude pulse which will switch fully a device (or pixel). These values, and the difference between them (the partial switching width), are of critical importance in the design of ferroelectric liquid crystal devices and addressing schemes. For a simple digital multiplexed scheme (i.e. no grey scale), it is important that the applied switching pulses are sufficient to switch the device fully and that the data being received by non-selected lines do not cause any switching. Additionally it is generally desirable that any required switching speed (defined for full switching) be achieved at the lowest possible drive voltage, both to lower the cost of display system construction and to minimize power consumption. Alternatively, for a device which will use the partially switched multi-domain states to achieve analogue grey scale in a display, it is desirable to obtain a well defined partial switching width. Clearly any variation in the partial switching width over the area of a display would lead to poor uniformity. Thus we can define the switching properties we might aim for: (i) minimum pulse width/amplitude for full switching; (ii) narrow partial switching width for maximum digital multiplexability; (iii) well defined and controllable partial switching regime for grey scale capability.

3. Approaches

The ways in which the switching time and width can be controlled break into three possible categories: (i) material optimization; (ii) cell construction; (iii) addressing scheme.

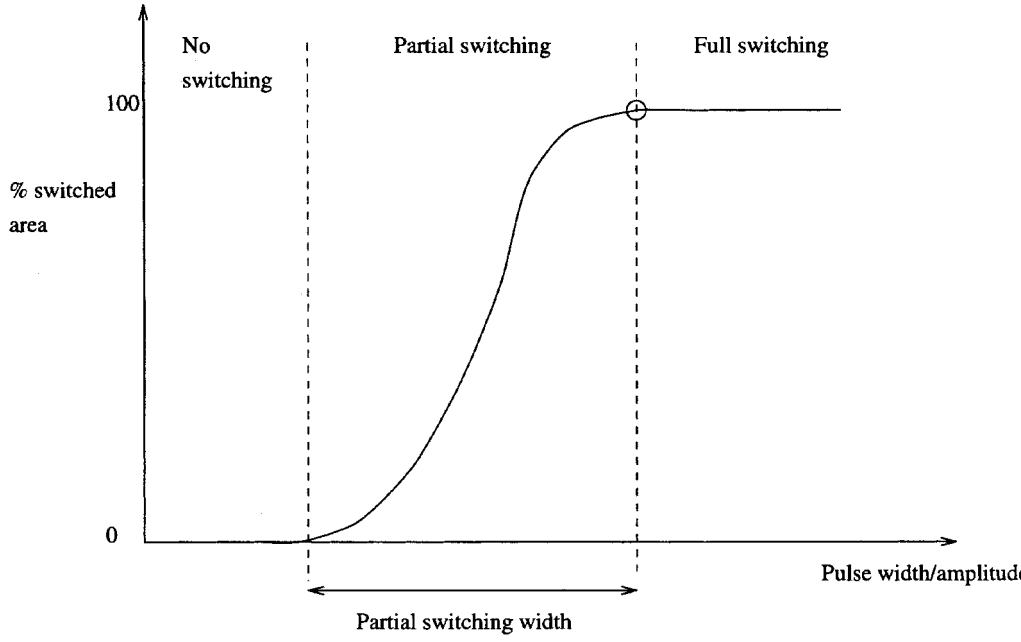

Figure 1. Schematic illustration of switching for a ferroelectric liquid crystal device, showing the 'no switching', 'partial switching' and 'full switching' regimes.

The first of these categories is generally associated with attempts to minimize the material viscosity. Other ways to improve the speed through material modification, e.g. increased spontaneous polarization, are less attractive due to other problems which are introduced (e.g. the formation of twisted states, and reverse switching effects). The second approach has also been studied, and development has concentrated on the optimization of surface alignment techniques for fast switching. *It is a particular surface alignment modification which is considered in this work*. Optimization of addressing schemes has also led to improved switching speeds, with the Joers–Alvey scheme [4] and Maltese's schemes [5] being particularly successful. None of these previously studied techniques controls the uniformity of domain switching over the area of a display panel. There has, however, been previous work which has used local cell thickness variation to control the switching threshold voltage in a ferroelectric liquid crystal device, and hence influence the switching process to aid grey scale [6], although the physical mechanisms operating are not discussed fully.

4. Our approach

As there are requirements for both improved switching speed (particularly for low voltage addressing) and partial switching width control (minimization for digital multiplexability, control for grey scale), a way of influencing the switching in a well defined way is required. Because the switching takes place through the formation and evolution of domains it is specifically this we have sought to control. As the domain wall velocity appears to be a material parameter (related to its viscosity), it is the number of domains formed which we have aimed to engineer.

Domains normally form at the same places each time a device is switched, indicating that they are seeded in some way [7]. Some of the seed sites can be identified, e.g. spacer beads and dirt particles. There are however a large number of randomly distributed sites in any given device at which domains nucleate. While statistically a reasonably uniform switching process takes place provided there are a large number of such sites, the sources of many seed sites are difficult to identify, and appear to be beyond our control. Additionally on the length scale of a pixel, the seeds are often not uniform enough. Careful investigation of a cell either before or after filling shows no discernible feature at many of the sites at which domains nucleate in a repeatable way. Additionally the domains do not all nucleate at the same time or at all voltages, complicating the nature of the switching. The latter point is illustrated in figure 2 (unseeded region), which shows that for a typical cell (SCE8) driven at low voltages (< 10 V) the total number of domains nucleating increases linearly with applied voltage.

Generally it is the sites which can be observed (spacer beads, etc.) which nucleate first and at the lower voltages. This has prompted us to investigate defect seeding with deliberately introduced features. The features

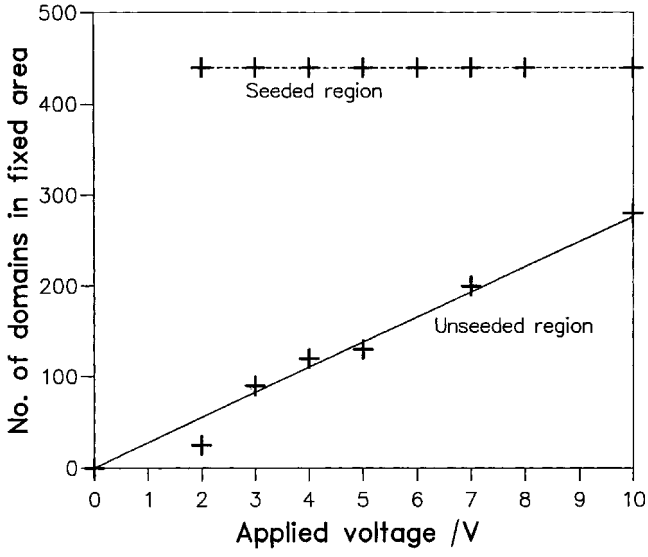

Figure 2. The number of domains nucleated in a fixed area of a test cell containing both seeded and unseeded regions. An area without seeds shows an approximately linear increase of domain density with applied pulse voltage; the seeded area, however, has an effectively constant domain density defined by the number of seed points.

investigated have been lines and dots, representing the introduction of line and point seeds. These features have sizes on the micron scale, and are therefore of similar size to the observable seed points. Results have proved very interesting.

5. Cell construction

The assembly of our test cells is very simple. They are made with standard 1·1-mm-thick ITO coated glass, onto which polyimide spacers of 2 μm thickness are deposited. A thin surface aligning layer of polyimide is also coated onto the surfaces, and this is lightly rubbed. The cells are assembled with the rubbing directions parallel, and capillary filled with SCE8 in the isotropic phase. Cooling to room temperature over about 1 h then forms a reasonable alignment.

To form seed points and lines, a photoresist layer of around 0·5 μm thickness is deposited onto the ITO (on one of the cell surfaces). This is then exposed through a suitable mask, developed and hard baked, before the alignment layer is coated onto the surface. The features we have studied have been: (i) 0·5-μm-high by 5-μm-wide lines in the alignment direction; (ii) 0·5-μm-high by 5-μm-wide lines perpendicular to the alignment direction; (iii) 0·5-μm-high by 5-μm-diameter dots. Dimensions given are approximate, and the features have a round top profile.

6. Alignment

The alignment quality of devices with the surface features is as good as that of those with a standard low pre-tilt rubbed polymer alignment. In the case of the device with an array of dots, the alignment is in fact better. Our devices generally show a number of zig–zag defects [8] (separating C1 and C2 regions [9]), but there are no zig–zags present in the regions with the dots. Therefore, we conclude that the dots form seed points for the C1 to C2 transition during cooling, leading to a uniform appearance.

7. Switching

The influence of the lines on the switching process is minimal. They do appear to have a pinning effect on domain wall movement, and can cause a degree of bias towards one state. They do not however appear to help us control the switching process in the desired ways, although the potential for controlled pinning of domain wall movement may be useful at pixel boundaries and for separation of sub-pixellated regions within pixels.

The dots, however, have a very significant effect on the switching process, causing the controlled seeding of domains. This seeding takes place uniformly from the array of dots at quite low voltages, therefore speeding up the switching significantly for small pulses. An image of the switching taking place, showing regions both with and without the dots is shown in figure 3. The region to the left shows the array of dots, each of which has nucleated a domain which is subsequently growing. The region to the right shows the few domains nucleated at random points in an untreated area of the cell. There are a number of important points to note about this.

(i) Almost every dot has seeded a domain, and because of the density of dots (which in this case are on 15 μm centres) these far outweigh the random naturally nucleated domains in the untreated region.

(ii) This significantly increases the switching speed, which is evident from the image as the domains in the treated region have almost coalesced, whereas those in the untreated region are few and far apart.

(iii) The domains in the treated region are of quite uniform size. This indicates that they effectively all seeded in a very narrow space of time, whereas those in the untreated region appear to nucleate over a wider time window and therefore have a broader size distribution.

The above points lead to a well defined partial switching width.

The switching times in the treated and untreated regions are shown in figure 4. This is for a simple

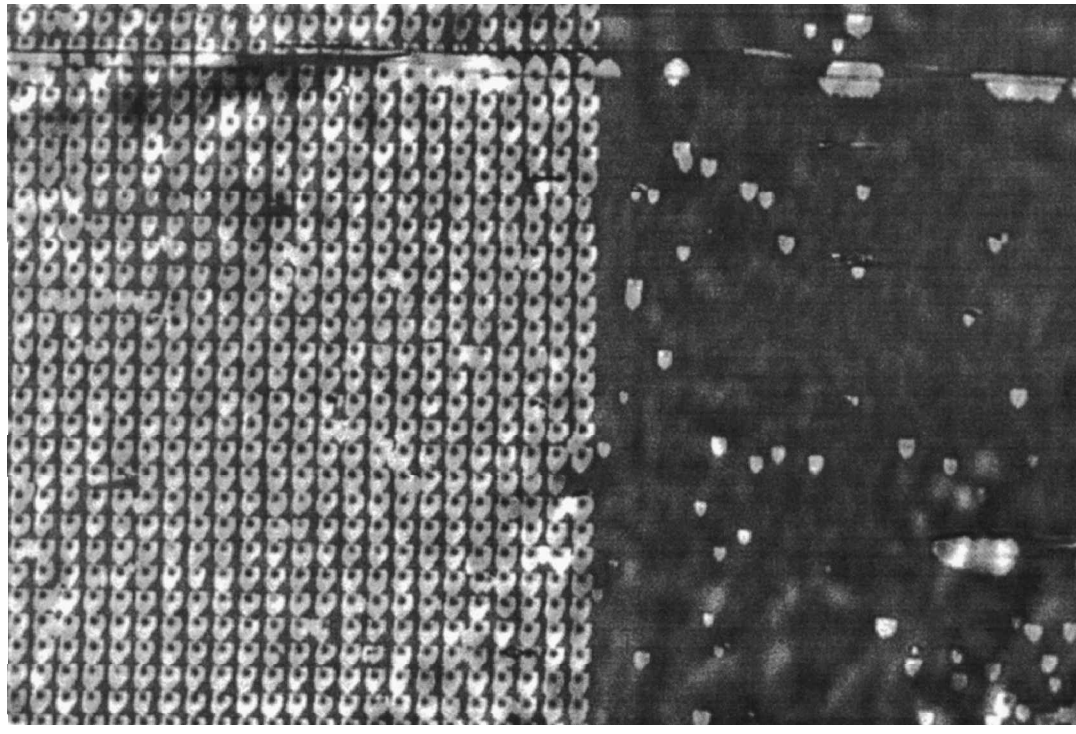

Figure 3. Illustration of switching in a ferroelectric liquid crystal device containing both seeded (left half) and unseeded (right half) regions. The much higher domain density and improved uniformity in the seeded region is apparent.

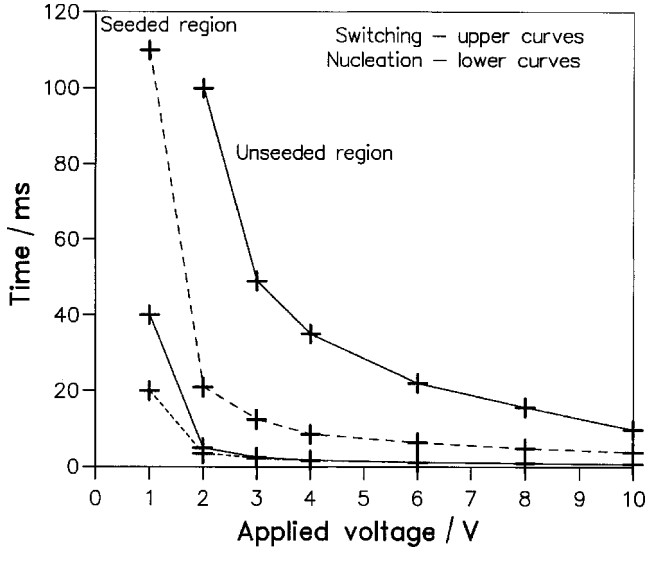

Figure 4. The measured times for nucleation and switching in the seeded (dashed lines) and unseeded (continuous lines) regions. Nucleation times are similar over a wide voltage range; the switching times are, however, significantly shorter in the seeded region.

switching monopolar pulse, starting from a relaxed state. It is interesting to note that the nucleation time is approximately the same in both regions. As nucleation is defined as the time at which domains are first observed, this indicates that the deliberately introduced seeds are causing domain nucleation in the same way as the most easily nucleated random sites. The total switching times are, however, significantly different. At very low drive voltages (2 V) the switching time for the treated region is a factor of 4 to 5 times less than that for the untreated region. There is an improvement at all moderate voltages, with the treated region being a factor of 2 faster at 10 V. This evolution in relative switching times occurs because in the untreated region the number of nucleated domains increases with increasing drive voltage, whereas in the treated region it is effectively constant. The total number of domains nucleated is shown by the dashed line in figure 2, and it is seen that this is independent of applied voltage.

The effect of the deliberate seeding can also be well illustrated by observing the switched area as a function of pulse duration. This is shown in figure 5, where the decreased partial switching width in the treated region is evident.

8. Mechanisms of seeding

Clearly the features we have introduced are large relative to the cell gap ($\approx 0{\cdot}25d$) and it might be argued that the areas over the seeds switch first due to the narrower cell gap in these regions. This, however, cannot

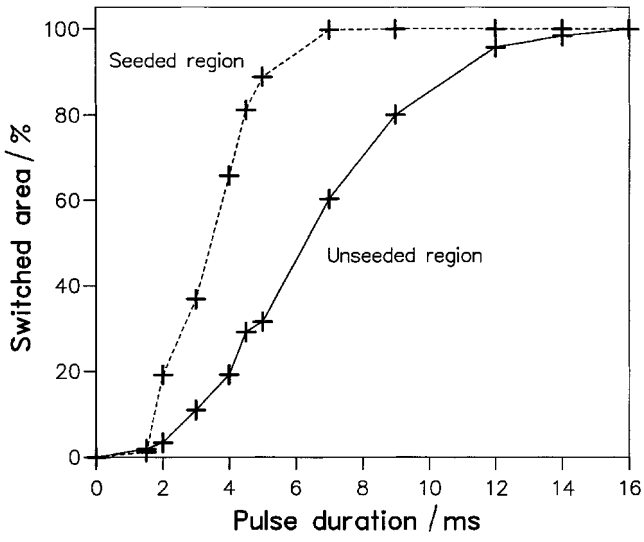

Figure 5. Final switched area as a function of pulse duration for a single 5 V monopolar pulse. The steeper switching curve and narrower partial switching width in the seeded region are evident.

be the key to the mechanism, as constructing a thinner cell or a cell with a uniform 0·5-μm-thick dielectric layer covering a significant area of one surface does not result in uniform switching over the whole area. We have also observed that 'linear' features, of the same height as the dots, did not nucleate domains. Thus it is not the cell gap change in the region of the seed points, but the shape of the introduced features which is of critical importance for nucleation.

A more reasonable explanation is that the features are causing a local perturbation in the smectic layer structure or/and director profile to take place as the material is cooled into the ferroelectric liquid crystal phase. This in turn lowers the effective anchoring energy at the chevron interface, thus seeding a nucleation point. What is not yet understood is the precise requirement for size and profile of the introduced features needed to cause a suitable perturbation. For example, there may be a critical slope in the feature profile at which domain wall pinning rather than nucleation occurs, and there will certainly be a critical density beyond which the seed points effectively merge and no longer nucleate domains.

9. Applications

As demonstrated here, an array of deliberately introduced seed points has a significant effect on switching in ferroelectric liquid crystals. *The high density array used causes nucleation to occur over a narrow time window, an increase in switching speed and a reduction in partial switching width*. Clearly the improvement in low voltage switching speed is of considerable interest in the development of low drive voltage displays using these materials. In addition, the narrower switching width which has resulted from creating a dense array of domain nucleation points has potential for improving the multiplexability of displays. Additionally this approach introduces flexibility in the control of the switching processes, and the possibility of engineering switching speed and width, etc. Here we have formed an array of relatively large seeds, but through control of both seed size and density there are a number of interesting possibilities.

(i) Increasing the density of seeds would narrow the partial switching width, as the more dense the seed points, the fewer domains have to grow to reach the switched state.

(ii) Varying the amplitude of seeds may allow control of the nucleation time. This would be particularly so if the natural density of seed points could be made low.

(iii) A low but well defined density of seeds may lead to a well defined and controlled partial switching regime, and therefore be useful for grey scale devices.

(iv) By combining an array of dots as seed points and lines as pinning sites it should be possible significantly to increase the partial switching width.

10. Conclusions

We have developed a way of controlling the domain switching in ferroelectric liquid crystal devices through the introduction of an array of seed points on one of the cell surfaces. This has allowed the decrease of switching times for low voltage addressing in a ferroelectric liquid crystal test cell. There is a clear route through these techniques to the engineering of switching speeds and the partial switching regime, and particularly of improved switching speeds for low drive voltage schemes. The techniques would be relatively easy to reproduce on a large scale using either photolithographic or printing techniques.

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